A THERMAL CONDUCTING TRENCH IN A SEMICONDUCTOR STRUCTURE AND METHOD FOR FORMING THE SAME

RELATED APPLICATION

[0001] The application is a continuation application of co-pending U.S. Patent Application, Serial No. 09/791,054, filed February 21, 2001, PAT 6,624,045 by applicants, Chunlin Liang and Brian S. Doyle, entitled "A Thermal Conducting Trench in a Semiconductor Structure and Method for Forming the Same;" which is a divisional application of co-pending U.S. Patent Application, Serial No. 08/829,860, filed on March 31, 1997, PAT 6,222,259 by applicants, Chunlin Liang and Brian S. Doyle, entitled "A Thermal Conducting Trench in a Semiconductor Structure and Method for Forming the Same."

BACKGROUND

Field

[0002] The invention relates generally to the field of semiconductor devices and, more particularly, to dissipating heat generated by the operation of such devices.

Description of Related Art

[0003] One goal of complementary metal oxide semiconductors (CMOS) in very large scale integration (VLSI) and ultra large scale integration (ULSI) is to increase chip density and operation speed. However, with increased chip density and operation speed, CMOS power consumption is also increased dramatically. It is expected that the power consumption of a high performance microprocessor will increase from several watts currently to approximately several hundred watts in the near future. The heat generated from this power consumption will raise chip temperature dramatically and degrade circuit performance and reliability. Therefore, reducing chip operation temperature is of great importance for current as well as future VLSI and ULSI technology.

[0004] To date, reduction of chip temperature is accomplished in two ways: 1) Lowering the power consumption, and 2) improving heat dissipation to the ambient environment. The first method is the preferred approach. A